

REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-3, 6, 9, and 10 under 35 USC § 102 (b) as being anticipated by Zhu (U.S. Patent No. 6,133,079); and claims 4, 7, and 11 under 35 USC § 103 (a) as being unpatentable over Zhu (U.S. Patent No. 6,133,079) in view of Merrill (U.S. Patent No. 5,610,433). The rejections and objections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-4, 6, 7, and 9-11.

2. Claims 1-3, 6, 9, and 10 have been rejected under 35 USC § 102 (b) as being anticipated by Zhu (U.S. Patent No. 6,133,079). The applicant respectfully disagrees with this rejection and the reasoning thereof.

Zhu teaches a reduce capacitance inductor as shown in Figures 4-7 and described in column 4, line 33, through column 5, line 33. As shown in Figure 4 and described in the corresponding text, the inductor region 22 includes an inductor coil 60 (which is formed on second and third metalization layers 57 and 59), a first IMD (inter-metal dielectric) 55, a second IMD 58, an ILD (inter-layer dielectric) 52, a FOX (field oxide) layer 50, a p-well 28, an n-region 24, and a substrate 20.

As shown in Figures 5-7, three serially coupled capacitors are formed between the inductive coil 60 and the substrate 20. The equivalent circuit is shown in Figure 7.

Thus, the inductor of Zhu, to achieve lower capacitance, includes multiple dielectric layers (IMD 1, IMD 2, and ILD), and a field oxide layer (FOX), a p-well 28, and an n-region 24.

Claim 1 claims an on-chip inductor consisting of: at least one dielectric layer; at least one conductive winding on the at least one dielectric layer; and P-well having a major surface parallel to a major surface of the dielectric layer.

As stated, in part, in MPEP § 2111.03, the transitional phrase “consisting of” excludes any element, step, or ingredient not specified in the claim. Since claim 1 includes the transitional phrase “consisting of” the claim excludes elements other than the at least one dielectric layer, the at least one conductive winding, and the P-well; Zhu’s inductor, which includes more elements (as listed above) than that of claim 1, does not anticipate the inductor of claim 1.

The same reasoning applies to distinguish claims 2, 3, 6, 9 and 10 over the anticipation rejection based on Zhu.

3. Claims 4, 7, and 11 have been rejected under 35 USC § 103 (a) as being unpatentable over Zhu (U.S. Patent No. 6,133,079) in view of Merrill (U.S. Patent No. 5,610,433). The applicant respectfully disagrees with this rejection and the reasoning thereof.

Claim 4 claims the on-chip inductor of claim 1 further consists of: the at least one dielectric layer includes a plurality of layers; and the at least conductive winding includes a plurality of windings on the plurality of layers.

The inductor of Zhu includes a plurality of dielectric layers (IMD 1, IMD 2, ILD), a field oxide (FOX) layer, a p-well 28, and an n region 24, which is more elements than are included in claim 4. Adding the additional teaches of Merrill (i.e., windings on multiple layers) to Zhu does not render claim 4 obvious.

Claim 7 claims the on-chip inductor of claim 1 further consists of: a secondary winding magnetically coupled to the conductive winding. Since the inductor of Zhu does not anticipate claim 1, the further limitation of further consisting of a secondary winding does not render claim 7 obvious.

The same reasoning applies to distinguish claim 11 over the same rejection.

For the foregoing reasons, the applicant believes that claims 1-4, 6, 7, and 9-11 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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